REMARKS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 242-274 are pending; Claims 243-244 have been amended; Claims 245-274 are newly added.

Response to Examiner's Arguments at point 13

Even though a capacitance can be produced by a dielectric layer between metal layers, Towle et al. fail to teach the capacitance can be used for a capacitor. Typically, resistance, capacitance and inductance are created in a circuit component in operation, but they are not used for a resistor, capacitor and an inductor, namely, a passive device. A passive device is designed by a human using the characteristics of resistance, capacitance and inductance created in a circuit. The circuit component in operation has resistance, capacitance and inductance, however, not used to be a resistor, capacitor and inductor, namely passive device. Even though Towle et al. teaches a structure 130 having multiple metal layers 114, 114' and 114" and multiple insulating layers 104, 104' and 104" therebetween, creating capacitances, Towle et al. fail to teach the capacitance can be used for a capacitor.

A functional limitation is an attempt to define something by what it does, rather than by what it is (e.g., as evidenced by its specific structure or specific ingredients). There is nothing inherently wrong with defining some part of an invention in functional terms. Functional language does not, in and of itself, render a claim improper. *In re Swinehart, 439 F.2d 210, 169 USPQ 226 (CCPA 1971).*

A functional limitation must be evaluated and considered, just like any other limitation of the claim, for what it fairly conveys to a person of ordinary skill in the pertinent art in the context in which it is used. A functional limitation is often used in

association with an element, ingredient, or step of a process to define a particular capability or purpose that is served by the recited element, ingredient or step.

Extracted from MPEP 2173.05(g)

In the above-mentioned reference from MPEP, a functional limitation should be evaluated and considered, just like any other limitation of the claim. Towle et al. fail to teach the structure 130 having multiple metal layers 114, 114' and 114" and multiple insulating layers 104, 104' and 104" therebetween, creating capacitances, may have a portion used to be a capacitor, namely a passive device, which can be deemed as a functional limitation. In the above-mentioned reference from MPEP, a functional limitation should be evaluated and considered, just like any other limitation of the claim. The Examiner would not focus too much on whether a structure having multiple metal layers and dielectric layers is disclosed, but instead reconsider the functional limitation.

Response to Claim Rejections under 35 U.S.C. 102 and 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 242 and 245-256

As previously presented, independent claim 242 is recited below:

242. A chip packaging method comprising:

joining a die and a substrate;

after said joining said die and said substrate, depositing a passive device over said substrate, wherein said passive device has a portion not over said die; and

separating said substrate.

Section I

Reconsideration of Claim 242 rejected under 35 U.S.C. 102(e) as being anticipated by US 2002/0,074,641 to Towle et al.

Applicants respectfully assert that the chip packaging method claimed in claim 242 patentably distinguishes over the citation by Towle et al. (US.2002/0074641).

Towle et al. teach that a chip packaging method comprises joining a die 214 and a substrate 202, and separating said substrate 202. ~ *See FIGS. 11-19, Par. 0027. lines 9-12 and Par. 0034, lines 7-11* ~

Towle et al. teach that a chip packaging method comprises depositing multiple patterned circuit layers 114, 114', 114", 120 and 120' and multiple insulating layers 104, 104' and 104" over the substrate 202. ~ *See FIGS. 1-8 and 11-19, Pars. 0023-0025, and Par. 0032, lines 1-3* ~ The laminated interconnector 130 having the patterned circuit layers 114, 114', 114", 120 and 120' and the insulating layers 104, 104' and 104" therebetween creates resistance, capacitance and inductance, but Towle et al. fail to teach, hint or suggest that the resistance, capacitance or inductance can be used for a resistor, capacitor or inductor, namely, a passive device. The Examiner would not focus too much on whether a structure having multiple patterned circuit layers and multiple insulating layers therebetween is disclosed or not, but instead reconsider the functional limitation. A functional limitation should be evaluated and considered, just like any other limitation of the claim. ~ *See MPEP 2173.05(g)* ~

It is believed that Towle et al. fail to teach, hint or suggest that the chip packaging method, after said joining said die 214 and said substrate 202, further comprises depositing a passive device over said substrate 202, wherein said passive device has a portion not over said die 214, as claimed in claim 242.

For at least the foregoing reasons, applicants respectfully submit independent claim 242 patently distinguishes over the prior art references, and should be allowed.

For at least the same reasons, dependent claims 245-256 patently define over the prior art as well.

Section II

Reconsideration of Claim 242 rejected under 35 U.S.C. 103(a) as being unpatentable over US 2002/0133943 to Sakamoto et al.

Applicants respectfully assert that the chip packaging method claimed in claim 242 patentably distinguishes over the citation by Sakamoto et al. (US 2002/0133943).

Sakamoto et al. teach that a chip packaging method comprises joining a die 52A and a substrate 51A, and depositing a passive device 52B over said substrate 51A, wherein said passive device 52B has a portion not over said die 52A. *~ See FIG 6 and Par. [0064] ~*

The Examiner considers that Sakamoto et al. disclose a chip packaging method comprises depositing metallization/trace (120) over a horizontal level (e.g. above chip) separated by dielectric layer that form a passive device (capacitance) over a substrate. *~ See lines 5-8 in point 6, on page 3, in the last Office Action mailed Jul. 13, 2006 ~* However, applicants can not find the reference number 120 in the specification or figures.

The Examiner considers that Sakamoto et al. disclose a chip packaging method comprises separating said substrate. ("singulated", Par. 0047) *~ See line 9 in point 6, on page 3, in the last Office Action mailed Jul. 13, 2006 ~* However, applicants can not find the teaching of "separating said substrate 51A" in the paragraph [0047].

Furthermore, Sakamoto et al. fail to teach, hint or suggest that said joining said die 52A and said substrate 51A are followed by said depositing said passive device 52B, as claimed in claim 242.

For at least the foregoing reasons, applicants respectfully submit independent

claim 242 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 245-256 patently define over the prior art as well.

Section III

Reconsideration of Claim 242 rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,867,499 to Tabrizi.

Applicants respectfully assert that the chip packaging method claimed in claim 242 patentably distinguishes over the citation by Tabrizi (US 6,867,499).

Tabrizi teaches that a chip packaging method comprises joining a die 520 and a substrate 510, and separating the substrate 510. *~See FIG 5 and col. 4, lines 9-13 ~*

Tabrizi teaches that a passive device may be added for the chip package. *~See col. 5, lines 1-4 ~* However, Tabrizi fails to teach, hint or suggest that the passive device has a portion not over said die 520, as claimed in claim 242.

The Examiner considers that since the placement of a capacitor to either the left or right of die would not modify the operation of the device and applicant has not disclosed that the placement is for any unobvious or critical reasons, the rearrangement of the capacitor would have been obvious since it has been held that the mere shifting of parts without providing modification to the device is obvious.

Applicants respectfully traverse the Examiner's opinions. The placement of a passive device having a portion not over a die leads the passive device far away from the die, and thereby the interference between the passive device and the die can be reduced, which is not anticipated by Tabrizi, in contrast to the placement of depositing the entire of an passive device over a die. As a result, the placement of a passive device having a portion not over a die modifies the operation of the chip structure.

For at least the foregoing reasons, applicants respectfully submit independent

claim 242 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 245-256 patently define over the prior art as well.

Response to Claims 243 and 257-268

As currently amended, independent claim 243 is recited below:

243. A chip packaging method comprising:

joining a die and a substrate;

after said joining said die and said substrate, depositing a passive device having a first connection point connected to said die;

after said depositing said passive device, depositing a metal bump connected to a second connection point of said passive device; and

separating said substrate.

Section I

Reconsideration of Claim 243 rejected under 35 U.S.C. 102(e) as being anticipated by US 2002/0,074,641 to Towle et al.

Applicants respectfully assert that the chip packaging method claimed in claim 243 patentably distinguishes over the citation by Towle et al. (US 2002/0074641).

Towle et al. teach that a chip packaging method comprises joining a die 214 and a substrate 202, depositing a metal bump 258, and separating said substrate 202. ~ *See FIGS. 11-19, Par. 0027, lines 9-12 and Par. 0034, lines 7-11* ~

Towle et al. teach that a chip packaging method comprises depositing multiple patterned circuit layers 114, 114', 114", 120 and 120' and multiple insulating layers 104, 104' and 104" over the substrate 202: ~ *See FIGS. 1-8 and 11-19, Pars. 0023-0025, and Par. 0032, lines 1-3* ~ The laminated interconnector 130 having the patterned circuit layers 114, 114', 114", 120 and 120' and the insulating layers 104,

104' and 104" therebetween creates resistance, capacitance and inductance, but Towle et al. fail to teach, hint or suggest that the resistance, capacitance or inductance can be used for a resistor, capacitor or inductor, namely, a passive device. The Examiner would not focus too much on whether a structure having multiple patterned circuit layers and multiple insulating layers therebetween is disclosed or not, but instead reconsider the functional limitation. A functional limitation should be evaluated and considered, just like any other limitation of the claim. *~ See MPEP 2173.05(g) ~*

It is believed that Towle et al. fail to teach, hint or suggest that the chip packaging method, after said joining said die 214 and said substrate 202, further comprises depositing a passive device having a first point connected to said die 214, as claimed in claim 243.

Furthermore, it is believed that Towle et al. fail to teach, hint or suggest that the chip packaging method, after said depositing said passive device, further comprises depositing said metal bump 258 connected to a second connection point of said passive device, as claimed in claim 243.

For at least the foregoing reasons, applicants respectfully submit independent claim 243 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 257-268 patently define over the prior art as well.

Section II

Reconsideration of Claim 243 rejected under 35 U.S.C. 103(a) as being unpatentable over US 2002/0133943 to Sakamoto et al.

Applicants respectfully assert that the chip packaging method claimed in claim 243 patentably distinguishes over the citation by Sakamoto et al. (US 2002/0133943).

Sakamoto et al. teach that a chip packaging method comprises joining a die 52A and a substrate 51A, and depositing a passive device 52B. *~ See FIG 6 and Par.*

[0064] ~

The Examiner considers that Sakamoto et al. disclose a chip packaging method comprises depositing metallization/trace (120) over a horizontal level (e.g. above chip) separated by dielectric layer that form a passive device (capacitance) over a substrate. *~ See lines 5-8 in point 6, on page 3, in the last Office Action mailed Jul. 13, 2006 ~* However, applicants can not find the reference number 120 in the specification or figures.

The Examiner considers that Sakamoto et al. discloses a chip packaging method comprises separating said substrate. ("singulated", Par. 0047) *~ See line 9 in point 6, on page 3, in the last Office Action mailed Jul. 13, 2006 ~* However, applicants can not find the teaching of "separating said substrate 51A" in the paragraph [0047].

Furthermore, Sakamoto et al. fail to teach, hint or suggest that said joining said die 52A and said substrate 51A is followed by said depositing said passive device 52B, as claimed in claim 243.

Furthermore, Sakamoto et al. fail to teach, hint or suggest that said passive device 52B has a first connection point connected to said die 52A, as claimed in claim 243.

Furthermore, Sakamoto et al. fail to teach, hint or suggest that the chip packaging method, after said depositing said passive device 52B, further comprises depositing a metal bump connected to a second connection point of said passive device 52B, as claimed in claim 243.

For at least the foregoing reasons, applicants respectfully submit independent claim 243 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 257-268 patently define over the prior art as well.

Section III

Reconsideration of Claim 243 rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,867,499 to Tabrizi.

Applicants respectfully assert that the chip packaging method claimed in claim 243 patentably distinguishes over the citation by Tabrizi (US 6,867,499).

Tabrizi teaches that a chip packaging method comprises joining a die 520 and a substrate 510, depositing a metal bump 21, and separating the substrate 510. ~ *See FIG 5 and lines 9-13, col. 4* ~

Tabrizi teaches that a passive device may be added for the chip package. ~ *See col. 5, lines 1-4* ~ However, Tabrizi fails to teach, hint or suggest that the passive device has a first connection point connected to said die 520, as claimed in claim 243.

Furthermore, it is believed that Tabrizi fails to teach, hint or suggest that the chip packaging method, after said depositing said passive device, further comprises depositing a metal bump 21 connected to a second connection point of said passive device, as claimed in claim 243.

For at least the foregoing reasons, applicants respectfully submit independent claim 243 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 257-268 patently define over the prior art as well.

Response to Claims 244 and 269-274

As currently amended, independent claim 242 is recited below:

244. A chip packaging method comprising:

providing a first die having a first top surface at a horizontal level;

providing a second die having a second top surface at said horizontal level;

depositing a passive device over said horizontal level, wherein said passive device has a portion not over said first and second dies; and

depositing a metal trace over said horizontal level, wherein said metal trace has a portion not over said first and second dies.

Section 1

Reconsideration of Claim 244 rejected under 35 U.S.C. 102(e) as being anticipated by US 2002/0,074,641 to Towle et al.

Applicants respectfully assert that the chip packaging method claimed in claim 244 patentably distinguishes over the citation by Towle et al. (US 2002/0074641).

Towle et al. teach that a chip packaging method comprises providing a first die (214, left side) having a first top surface at a horizontal level; providing a second die (214, right side) having a second top surface at said horizontal level; and depositing a metal trace 114, 114', 114", 120 or 120' over said horizontal level, wherein said metal trace 114, 114', 114", 120 or 120' has a portion not over said first and second dies 214. *~ See FIGS. 1-8 and 11-19, Pars. 0023-0025, and Par. 0032, lines 1-3 ~*

The laminated interconnector 130 having the patterned circuit layers 114, 114', 114", 120 and 120' and the insulating layers 104, 104' and 104" therebetween creates resistance, capacitance and inductance, but Towle et al. fail to teach, hint or suggest that the resistance, capacitance or inductance can be used for a resistor, capacitor or inductor, namely, a passive device. The Examiner would not focus too much on whether a structure having multiple patterned circuit layers and multiple insulating layers therebetween is disclosed or not, but instead reconsider the functional limitation. A functional limitation should be evaluated and considered, just like any other limitation of the claim. *~ See MPEP 2173.05(g) ~*

It is believed that Towle et al. fail to teach, hint or suggest that the chip packaging method comprises depositing a passive device over said horizontal level,

wherein said passive device has a portion not over said first and second dies 214, as claimed in claim 244.

For at least the foregoing reasons, applicants respectfully submit independent claim 244 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 269-274 patently define over the prior art as well.

Section II

Reconsideration of Claim 244 rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,867,499 to Tabrizi.

Applicants respectfully assert that the chip packaging method claimed in claim 244 patentably distinguishes over the citation by Tabrizi (US 6,867,499).

Tabrizi teaches that a chip packaging method comprises providing a first die 520 having a first top surface at a horizontal level; and depositing a metal trace 560 over said horizontal level, wherein said metal trace 560 has a portion not over said first die 520. *~ See FIG. 5 and col. 4, lines 41-44 ~*

Tabrizi teaches that a passive device may be added for the chip package. *~ See col. 5, lines 1-4 ~* However, Tabrizi fails to teach, hint or suggest that the passive device has a portion not over said die 520, as claimed in claim 244.

The Examiner considers that since the placement of a capacitor to either the left or right of die would not modify the operation of the device and applicant has not disclosed that the placement is for any unobvious or critical reasons, the rearrangement of the capacitor would have been obvious since it has been held that the mere shifting of parts without providing modification to the device are obvious.

Applicants respectfully traverse the Examiner's opinions. The placement of a passive device having a portion not over a die leads the passive device far away from

the die, and thereby the interference between the passive device and the die can be reduced, which is not anticipated by Tabrizi, in contrast to the placement of depositing the entire of an passive device over a die. As a result, the placement of a passive device having a portion not over a die modifies the operation of the chip structure.

For at least the foregoing reasons, applicants respectfully submit independent claim 244 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 269-274 patently define over the prior art as well.

CONCLUSION

Some or all of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

Sincerely yours,

/ Winston Hsu /

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)